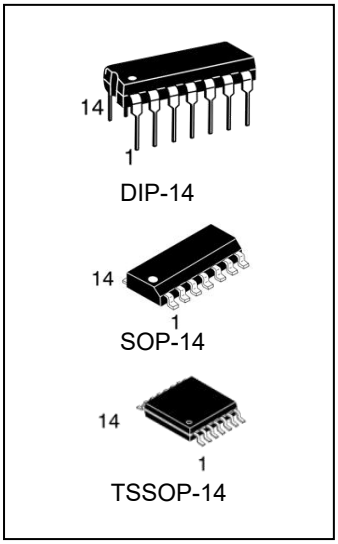
74HC08 4-way 2-input AND gate

Overview

The 74HC08 is a high-speed CMOS circuit that is pin-compatible with the low-power Schottky TTL (LSTTL) series. The 74HC08 complies with JEDEC standard no.7A. The 74HC08 implements a 2-input AND gate function.

Its main features are as follows:

- Compatible with JEDEC standard no.8-1A
- ESD protection
  HBM EIA/JESD22-A114-A exceeds 2000V
  MM EIA/JESD22-A115-A exceeds 200V
- Wide working environment temperature range, -40~+85℃
- Package type:DIP-14/SOP-14/TSSOP-14



Product ordering information

Product name	Encapsulation	Print name	Package	Packing quantity
74HC08N	DIP-14	74HC08	Tube	1000 pcs/box
74HC08M/TR	SOP-14	74HC08	Braid	2500 pcs/tray
74HC08MT/TR	TSSOP-14	HC08	Braid	2500 pcs/tray

Function box

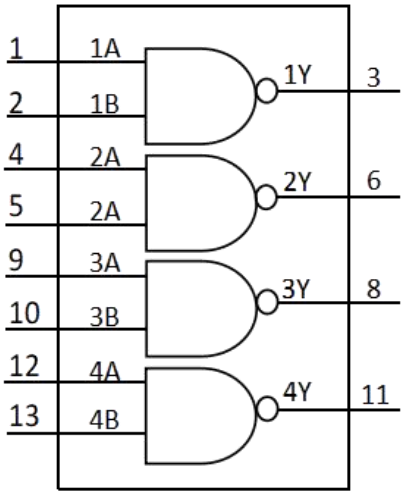


Figure 1: Functional block diagram

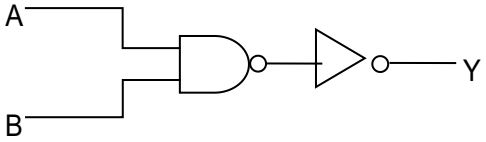


Figure 2: Single logical door frame

Pinout description

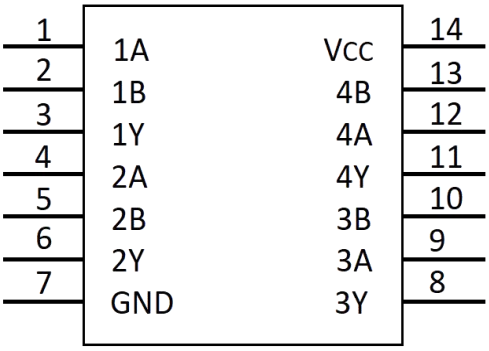


Figure 3: Pinout

Pin description

Pin	Symbol	Function	Pin	Symbol	Function
1	1A	Data input	8	3Y	Data output
2	1B	Data input	9	3A	Data input
3	1Y	Data output	10	3B	Data input
4	2A	Data input	11	4Y	Data output
5	2B	Data input	12	4A	Data input
6	2Y	Input and output	13	4B	Data input
7	GND	Ground（0V）	14	Vcc	Supply voltage

Truth table:

Input		Output
nA	**nB**	**nY**
L	L	L
L	H	L
H	L	L
H	H	H

Absolute maximum ratings （Unless otherwise specified, Tamb=25℃， GND=0V）

Parameter name	Symbol	Test conditions		Minimum	Typical	Maximum	Unit
Supply voltage	V_{CC}	—		-0.5	—	+7	V
Input clamp current	I_{IK}	V_O < -0.5V or V_O > V_{CC}+0.5V		—	—	±20	mA
Output clamp current	I_{OK}	V_O= -0.5V ~ V_{CC}+0.5V		—	—	±20	mA
Output current	I_O	—		—	—	±25	mA
V_{CC} or **GND** current	I_{CC}, I_{GND}	—		—	—	±50	mA
Storage temperature	T_{STG}	—		-65	—	+150	℃
Soldering temperature	T_L	10 seconds	DIP	—	245	—	℃
			SOP	—	245	—	

Note: Extreme parameters refer to the limit values that cannot be exceeded under any conditions. If the limit values are exceeded, physical damage such as product degradation may occur; at the same time, the chip cannot be guaranteed to work properly when the limit parameters are close to the limit.

Recommended conditions of use

Parameter name	Symbol	Test conditions	Minimum	Typical	Maximum	Unit
Supply voltage	V_{CC}		2.0	5.0	6.0	V
Input voltage	V_I		0	-	V_{CC}	V
Output voltage	V_O		0	-	V_{CC}	V
Input rise and fall time	tr,tf	V_{CC}=2.0V	-	-	1000	ns
		V_{CC}=4.5V	-	6.0	500	ns
		V_{CC}=6.0V	-	-	400	ns
Working temperature	Tamb		-40	+25	+85	℃

DC Parameters 1 (Unless otherwise specified, Tamb = 25℃,GND = 0V)

Parameter name	Symbol	Test conditions		Minimum	Typical	Maximum	Unit
Input high level voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
Input low level voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
Output high level voltage	V_{OH}	Vi=V_{IH} or V_{IL}	V_{CC}=2.0V , I_O=-20uA	1.9	2.0	-	V
			V_{CC}=4.5V , I_O =-20uA	4.4	4.5	-	V
			V_{CC}=6.0V , I_O =-20uA	5.9	6.0	-	V
			V_{CC}=4.5V , I_O =-4.0mA	3.98	4.32	-	V
			V_{CC}=6.0V , I_O =-5.2mA	5.48	5.81	-	V
Output low level voltage	V_{OL}	Vi=V_{IH} or V_{IL}	V_{CC}=2.0V , I_O =20uA	-	0	0.1	V
			V_{CC}=4.5V , I_O =20uA	-	0	0.1	V
			V_{CC}=6.0V , I_O =20uA	-	0	0.1	V
			V_{CC}=4.5V , I_O =4.0mA	-	0.15	0.26	V
			V_{CC}=6.0V , I_O =5.2mA	-	0.16	0.26	V
Input leakage current	I_{LI}	Vi=V_{CC} or GND, V_{CC}=6.0V		-	-	±0.1	uA
Quiescent current	I_{CC}	Vi=V_{CC} or GND, V_{CC}=6.0V, I_O=0 uA		-	-	2.0	uA

DC Parameters 2 (Unless otherwise specified, Tamb= -40 ~ +85 °C, GND=0)

Parameter name	Symbol	Test conditions		Minimum	Typical	Maximum	Unit
Input high level voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
Input low level voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
Output high level voltage	V_{OH}	Vi=V_{IH} or V_{IL}	V_{CC}=2.0V , I_O =-20uA	1.9	-	-	V
			V_{CC}=4.5V , I_O =-20uA	4.4	-	-	V
			V_{CC}=6.0V , I_O =-20uA	5.9	-	-	V
			V_{CC}=4.5V , I_O =-4.0mA	3.84	-	-	V
			V_{CC}=6.0V , I_O =-5.2mA	5.34	-	-	V
Output low level voltage	V_{OL}	Vi=V_{IH} or V_{IL}	V_{CC}=2.0V , I_O =20uA	-	-	0.1	V
			V_{CC}=4.5V , I_O =20uA	-	-	0.1	V
			V_{CC}=6.0V , I_O =20uA	-	-	0.1	V
			V_{CC}=4.5V , I_O =4.0mA	-	-	0.33	V
			V_{CC}=6.0V , I_O =5.2mA	-	-	0.33	V
Input leakage current	I_{LI}	Vi=V_{CC} or GND, V_{CC}=6.0V		-	-	±1.0	uA
Quiescent current	I_{CC}	Vi=V_{CC} or GND, V_{CC}=6.0V, I_O=0 uA		-	-	20	uA

AC Parameters 1

(Unless otherwise specified, Tamb= 25℃,GND=0, tr = tf =6.0ns, CL=50pF; see figure 4, figure 5)

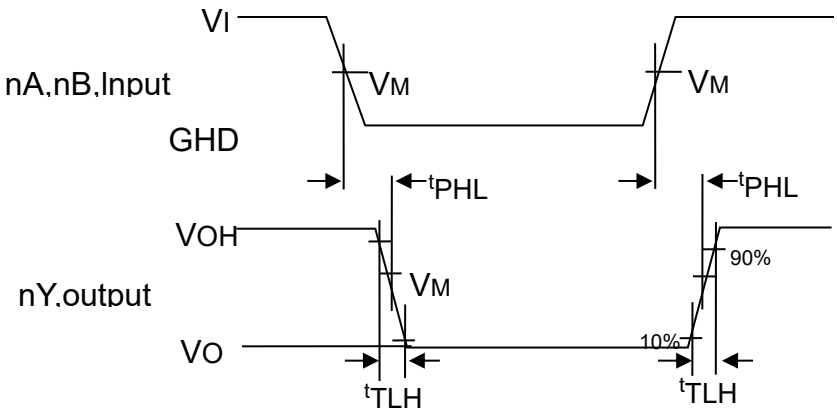
Parameter name	Symbol	Test conditions	Minimum	Typical	Maximum	Unit
nA,**nB** to **nY** propagation delay	t_{PHL}/t_{PLH}	V_{CC}= 2.0V	-	25	90	ns
		V_{CC}= 4.5V	-	9	18	ns
		V_{CC}= 6.0V	-	7	15	ns
Transition time	t_{THL}/t_{TLH}	V_{CC}= 2.0V	-	19	75	ns
		V_{CC}= 4.5V	-	7	15	ns
		V_{CC}= 6.0V	-	6	13	ns

AC Parameters 2

(Unless otherwise specified, Tamb= -40 ~ +85 °C ,GND=0,tr = tf =6.0ns,CL=50pF; see figure 4, figure 5)

Parameter name	Symbol	Test conditions	Minimum	Typical	Maximum	Unit
nA, **nB** to **nY** propagation delay	t_{PHL}/t_{PLH}	V_{CC}= 2.0V	-	-	115	ns
		V_{CC}= 4.5V	-	-	23	ns
		V_{CC}= 6.0V	-	-	20	ns
Transition time	t_{THL}/t_{TLH}	V_{CC}= 2.0V	-	-	95	ns
		V_{CC}= 4.5V	-	-	19	ns
		V_{CC}= 6.0V	-	-	16	ns

AC waveform



74HC08: VM = 50%; VI = GND to VCC

Figure 4: Delay waveform from input (nA, nB) to output (nY)

AC test chart

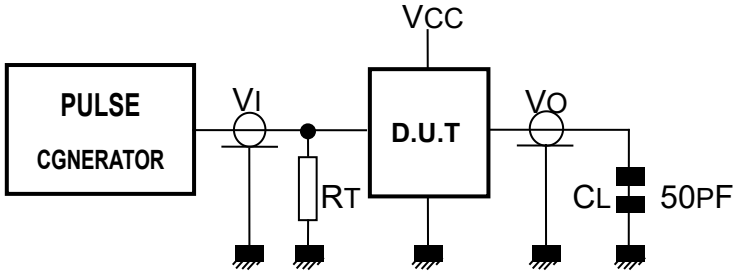


Figure 5: AC test diagram

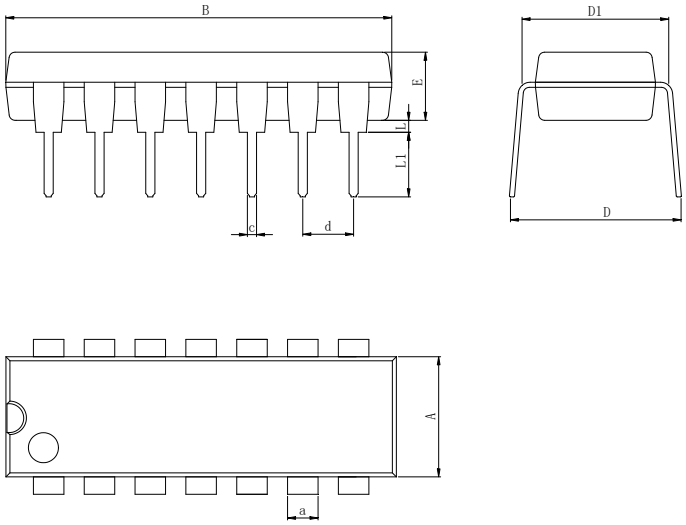
Note:

RT: The terminal resistance must match the output impedance of the signal generator.

CL: Load capacitance must include the probe capacitance of the fixture.

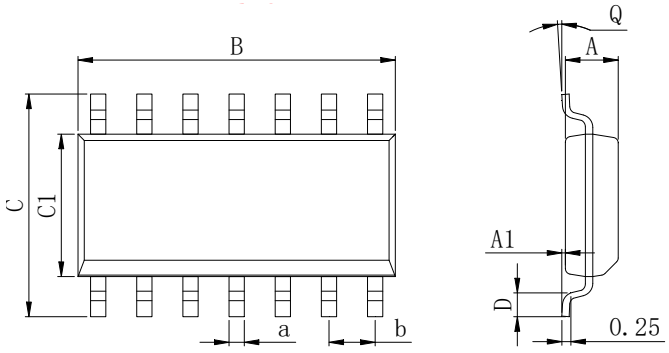
Package dimensions

DIP-14



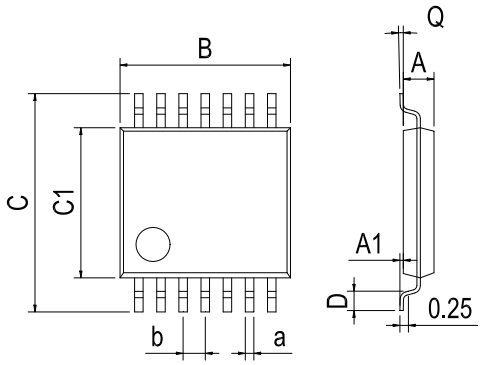
Dimensions In Millimeters(DIP-14)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision history

Date	Modify content	Page number
2015-3-18	New revision	1-9
2023-9-7	Updated pin soldering temperature, updated package, updated DIP-14 size, added extreme parameter notes.	1,2,6

Important statement:

Arima Semiconductor reserves the right to change the products and services provided without notice. Customers should obtain the latest relevant information before placing an order and verify whether the information is up to date and complete. Arima Semiconductor assumes no responsibility or obligation for any modified documents.

Customers who use Arima Semiconductor products for system design and machine manufacturing are responsible for complying with safety standards and taking safety measures. You will bear all the following responsibilities: Select the appropriate Arima Semiconductor product design for your application, verify and test the application: Ensure that your application meets the corresponding standards and any other safety, security or other requirements to avoid potential risks that may cause personal injury or property damage.

Huaguan Semiconductor products have not been approved for use in the fields of life support, military, aerospace, etc., and Huaguan Semiconductor will not be responsible for the consequences of the use of products in these fields. All problems and responsibilities caused by the use of the product beyond the applicable field by the user shall be borne by the user and shall have no liability to Huaguan Semiconductor. The user shall not claim any compensation from Huaguan Semiconductor based on the terms of this agreement.

Arima Semiconductor provides technical and reliability data (printed data sheets), design resources (including reference designs), application or other design advice, web tools, safety information and other resources on the performance of semiconductor products produced by Arima Semiconductor. No warranty is made, express or implied, without warranty of any kind. The use of testing and other quality control techniques is limited to the quality assurance scope of Arima Semiconductor. Not all parameters of every three devices need to be tested.

The documents and materials of Huaguan Semiconductor can only be used for the research and development of the products described in this document. You have no right to disclaim other Huaguan Semiconductor's property rights or any third-party intellectual property rights. It is strictly prohibited to use these resources. Other categories or displays, but full credit shall be given to any claims, damages, costs, losses and debts caused by Huaguan Semiconductor and its agents in the use of these resources, and Huaguan Semiconductor is not responsible for this.